QP CODE	2043511702

Reg. No | | | | | | | | | | |

DMI-ST. EUGENE UNIVERSITY

ZAMBIA

DEGREE EXAMINATION – DECEMBER 2024

Semester: IV 351HE24 COMPUTER SYSTEM ARCHITECTURE

Time: 3:00 Hours **Max. Marks: 100**

Answer any FIVE Questions (5 x 20 = 100 Marks)

1. a) With a neat block diagram, elaborate components of a digital computer. **(10 Marks)**

   b) Describe big endian and little endian with examples. **(10 Marks)**

2. a) Discuss concepts of stack organization implementation in 8086.Draw the diagrams. **(10 Marks)**

   b) Give a detailed account on instruction formats of 8086. **(10 Marks)**

3. a) Describe the concepts of pipelining with diagrams. **(10 Marks)**

   b) Draw a flowchart for Booth algorithm for multiplication and It shows the step by step multiplication of -5 and -7 using the same algorithm. **(10 Marks)**

4. a) Depict the Hardware organization of associative memory. State the applications, advantages and disadvantages. **(10 Marks)**

   b) Describe DMA data transfer with the help of a block diagram. **(10 Marks)**

5. a) Describe SIMD array processor with a diagram. **(10 Marks)**

   b) Elaborate on a typical example of a four-segment instruction pipeline in instruction pipeline

with a diagram. **(10 Marks)**

6. a) Explain in detail the classification of a computer based on On the Basis of Size and Capacity**. (10 Marks)**

   b) Give a detailed account on middleware and Firmware. State difference. **(10 Marks)**

7. a) Give a detailed explanation on signed magnitude addition and subtraction of numbers with the help of a table. Draw hardware implementation of the same. **(10 Marks)**

   b) Illustrate Algorithm for Floating Point Addition/Subtraction and compute addition of $X=1.3255X10^{19}$ and $y=1.652X10^{23}$ **(10 Marks)**